



# राष्ट्रीय प्रौद्योगिकी संस्थान जमशेदपुर

## National Institute of Technology Jamshedpur

Jamshedpur-831014, Jharkhand, India

(An Institution of National importance under MoE, Government of India)

इलेक्ट्रॉनिक्स एवं संचार इंजीनियरिंग विभाग / Department of Electronics and Communication Engg.

Advt. No.: NITJSR/ECE/2026/112

Date: 06-04-2026

### Advertisement for the post of Junior Research Fellow (JRF)

Applications are invited from Indian citizens for a temporary position of **Junior Research Fellow (JRF)** in the research project entitled “**Design and Development of a Low-Power, High-Speed FPGA-Based System for Real-Time Epileptic Seizure Detection**” sponsored by the Anusandhan National Research Foundation (ANRF), Government of India. The project will be implemented in the Department of Electronics and Communication Engineering, National Institute of Technology Jamshedpur, India.

Details:

|                                     |  |
|-------------------------------------|--|
| Title of the Project                | Design and Development of a Low-Power, High-Speed FPGA-Based System for Real-Time Epileptic Seizure Detection  |
| Funding Agency                      | Anusandhan National Research Foundation (ANRF), Government of India  |
| Name of the Post and no. of vacancy | JRF: 01  |
| Duration                            | The post is purely temporary and co-terminus with the project. Initial appointment will be for maximum 1 year which may be extended later or terminated earlier based on the performance.  |
| Fellowship                          | JRF: Rs. 37,000/- per month + HRA @ 20%  |
| Principal Investigator (PI)         | Dr. Kaushik Das<br>Assistant Professor, Department of Electronics and Communication Engineering<br>National Institute of Technology Jamshedpur<br><b>Email: kaushik.ece@nitjsr.ac.in, Mob: +91-7005728730</b>  |
| Essential Qualification             | M.E./M.Tech/MS in ECE/EIE Dept. with specialization in Digital VLSI, VLSI Signal Processing, or related areas, and a minimum of 60% marks (1st class) at both B.E./B.Tech. and M.E./M.Tech.  |
| Desirable Qualification             | Adequate knowledge of FPGA implementation, Verilog/ SystemVerilog, and MATLAB HDL Coder  |
| Age Limit                           | Should not exceed 35 Years as of last date of application. Age relaxations will be provided as per norms and to the candidates with relevant experiences.  |
| How to Apply                        | Eligible and interested candidates are encouraged to send their application as per the prescribed format along with self-attested copies of all supporting documents as a single PDF file through Email to the PI Dr. Kaushik Das ( <b>kaushik.ece@nitjsr.ac.in</b> ) mentioning email subject as “ <b>Application for the Post of JRF under ANRF-Sponsored Project</b> ”. For more information contact: <b>+91- 7005728730</b> .<br><b>Last date of receipt of applications is April 24, 2026 (5 PM).</b> |
| Project Tenure                      | 3 years  |

**Benefits of joining the post:** Candidates selected for the position can register for the Ph.D. program provided she/he satisfies the eligibility criteria for Ph.D. program in NIT Jamshedpur.

#### General Instructions:

1. Candidate should ensure their eligibility for the post before applying. Ineligible candidates will not be allowed. Shortlisted candidates will be called for interview. Please refer to the Institute website for updates, if any.
2. The assignment is purely temporary in nature and is co-terminus with the project.
3. No TA/DA will be paid for appearing in the interview and/or joining the position.
4. All the terms & conditions for this recruitment will be as per the guidelines of funding agency and NIT Jamshedpur. Institute reserves the right to cancel the recruitment without assigning any reason.
5. The selected candidate will be required to work in the Department of ECE, NIT Jamshedpur as full-time research fellow.
6. Original documents of age proof/certificates/degrees/mark sheets and other testimonials must be presented at the time of interview and joining (if selected) for verification.



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**Application for the Post of JRF in the project titled “Design and Development of a Low-Power, High-Speed FPGA-Based System for Real-Time Epileptic Seizure Detection”**

**Applicant's Details:**

|    |                         |   |                                     |
|----|-------------------------|---|-------------------------------------|
| 1. | Name (In Capital)       |   | PHOTO                               |
| 2. | Name of Father/Guardian |   |                                     |
| 3. | Mother's Name           |   |                                     |
| 4. | Gender                  |   |                                     |
| 5. | Address                 | Correspondence:                         | Permanent:                          |
| 6. | Contact Details         | Email ID:                               | Phone Number:                       |
| 7. | Age:                    | Date of Birth:                          | Age as on the closing date of Advt: |
| 8. | Nationality:            | Category: GEN/SC/ST/OBC (attach proof): |                                     |
| 9. | Languages Known         | Mother tongue:                          | Other languages:                    |

**10. Academic Records:**

**(Supporting documents should be submitted along with the application as a single PDF file)**

**(a) Qualifying Degree Details:**

| Degree/Certificate            | University/Board/College | Year | Subjects/Specialization | % Marks/CGPA | Class |
|-------------------------------|--------------------------|------|-------------------------|--------------|-------|
| 10 <sup>th</sup>              |                          |      |                         |              |       |
| 12 <sup>th</sup>              |                          |      |                         |              |       |
| BE/ B. Tech./ Graduation      |                          |      |                         |              |       |
| M. Tech./ME/MS                |                          |      |                         |              |       |
| Publication Details (if any): |                          |      |                         |              |       |

**(b) GATE scores:**

| Exams | Year Appeared | Scores | All India Rank | Validity Up to |
|-------|---------------|--------|----------------|----------------|
| GATE  |               |        |                |                |

11. M. Tech/ME/MS Dissertation Title:

12. BE/ B. Tech Project Title:

13. Any other relevant information:

14. Declaration: I hereby declare that the entries made in this application form are correct to the best of my knowledge and belief.

Place:

Date:

(Signature of the applicant)