Practice Problems: Basic Electronics EE1101-2020

1. What do you understand by a semiconductor? Differentiate between an insulator, conductor and semiconductor.
2. Explain the working of a PN junction diode. Define space charge region or depletion region.
3. What do you mean by Ideal diode & explain the V-I Characteristic of non Ideal diode in forward region, reverse region and breakdown region.
4. (a) How does the reverse saturation current of a p-n diode vary with temperature?
   (b) How does the diode voltage (at constant current) vary with temperature?
5. (a) Define dynamic resistance of a diode. Calculate the dynamic resistance *r* for a silicon diode at room temperature for a dc current of 1mA.

(b) Explain the transition capacitors C_T and the diffusion capacitance C_D of a diode. What is a varactor diode.

6. (a) Explain physical mechanism for avalanche breakdown in diodes.
   (b) Explain physical mechanism for Zener breakdown in diodes.
7. A silicon diode is operating at 25^oC with a forward bias of 0.6V and current of 0.5A. Calculate I_O. If current is held constant at 0.5A, what voltage will exist across the diode at the following temperatures (i) 75^oC, (ii) -45^oC ?
8. A silicon diode operates at a forward voltage of 0.4V. Calculate the factor by which the current will be multiplied when temperature is increased from 25 to 150^oC.
9. (a) A silicon diode has a reverse breakdown voltage V_B of 100V. Its reverse current I_R, is 1 μA at 22^oC when reverse voltage applied across the diode is 95V.
   (b) What is the diode's reverse saturation current at 22^oC?
   (c) How much current will flow through the diode when it is forward biased with 0.5V at room temperature? What will be the forward current at 0.5V forward bias when temperature raises 30^oC?
10. Calculate the barrier capacitance of a germanium p-n junction whose area is 1mm by 1mm and whose space charge thickness is 2×10^{-4} cm. The dielectric constant of germanium (relative to free space) is 16.
11. What does a dc load line drawn on diode's characteristic represent?
12. Explain with the aid of a sketch the use of a diode's characteristic and dc load line to determine the dc current that will flow through a diode when it is connected in series with a resistor and a dc supply.
    (b) (a) Explain how to obtain the dynamic characteristic from static volt-ampere curve of a diode. Draw the dc load line for (i) infinite load resistance, $R_L = \infty$, (ii) $R_L = 0$.
    (c) Define for a diode (i) static characteristic (ii) dynamic characteristic (iii) transfer or transmission characteristic.
    (d) What is the correlation between the dynamic and transfer characteristic?
14. For a Zener diode explains: Zener knee current I_{zk}, Zener test current and test voltage, and the dynamic impedance Z_z.
15. Explain briefly the two different mechanisms at work in Zener diodes below and above approximately 6V breakdown.
16. (a) Draw a circuit using Zener diode to regulate the voltage across the load. Explain its operation. Can this circuit regulate the variations input voltage? Explain.
    (b) Two p-n, Ge diodes are connected in series opposing. A 5V battery is imposed upon this series arrangement. Find the voltage across each junction at room temperature, Assume that the magnitude of the Zener voltage is greater than 5V. Note that the result is independent of reverse saturation current. Is it also independent of temperature?

17. If the magnitude of the Zener voltage is 4.9V, what be the current in the circuit? The reverse saturation current is 5μA.
18. Design a voltage regulator circuit to provide 12V across a load whose current varies from 5mA to 35mA. An unregulated 18V dc source is to be used. For Zener it is given that V_z = 12V at I_{zT} = 20mA. Determine:
    (a) The voltage dropping resistor and its power rating using an average value for I_L when $L_z = I_{zT}$.
    (b) Minimum power rating of the Zener diode.
    (c) The maximum value of I_{zk} to maintain reasonable voltage regulation when load current is at its maximum.
    (d) Assuming that for average Zener current of 20mA the Z_z = 10 ohms; calculate the approximate voltage variation and percent regulation expected from 5mA to 35mA variation in load current.
19. (a) A 10V Zener diode is operated at a reverse current of 5mA at room temperature of 20^{o}C. Determine its Zener voltage at temperature of 75^{0}C.Assume Zener temperature coefficient $\propto_z$ = 0.06% / ^{o}C.
    (b) Assuming the change in Zener voltage in part (a) is more than that can be tolerated, what change will take place at 75^{o}C if diode is operated at 40ma. Assume $\propto_z$ = 0.035% / ^{o}C in this case.
20. What would be the overall change in Zener voltage at 75^{o}C if two 5V Zener diodes were operated in series at a current of 4mA? Take V_z = 5V at 20^{o}C and $\propto_z$ = 0.005% / ^{o}C.
21. A 12V Zener operating at 5mA has dynamic impedance Z_z = 25 ohms. Calculate the change in Zener voltage for 1.5mA change in its current.
22. A Zener diode has Zener voltage 4V at room temperature. Will this increase or decrease or remain same when the temperature rises to 50^{o}C?
26. (a) Refer to fig.1 The avalanche diode regulates at 50V over a range of diode currents from 5 to 40 mA. The supply voltage V = 200V. Calculate R to allow voltage regulation from a load current I_L = 0 up to I_{max}, the maximum possible value of I_L. What is I_{max}?
    (b) If R is set as in part (a) and the load current is set at IL = 25 mA, what are the limits between which V may vary without loss of regulation in the circuit?

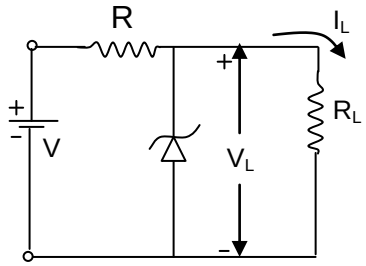


Fig 1

1. What do you mean by rectification? Explain the working of a half wave rectifier.
2. Define ripple factor, ratio of rectification and transformer utilization factor.
3. Show that the ripple factor for a half wave rectifier is 1.21. Also find the values of ratio of rectification and transformer utilization factor.
4. Derive the ripple factor for a full wave rectifier. Also find out the values of ratio of rectification and transformer utilization factor.
5. Define in words and as an equation the (i) dc current, I_{dc} (ii) DC voltage, V_{dc} (iii) ac current I_{rms}.
6. (a) Show that, for a half wave rectifier the following:
    (i) $I_{dc} = I_{av} = I_m/\pi$ (ii) $I_{rms} = I_m/2$
    (iii) $V_{dc} = V_m/\pi - I_{dc}(R_f + R_s)$.
    (b) Similarly, obtain the expressions for I_{dc}, V_{dc}, and I_{rms} for a full wave rectifier.

7. Define regulation. A power supply has 100% regulation. Is it a good power supply? Justify your answer.
8. Derive the regulation equation for a full-wave rectifier.
9. (a) Define PIV. What is the PIV for a full wave rectifier using ideal diodes for (i) circuit using two diodes, (ii) bridge circuit?
   (b) What is the PIV for a half-wave rectifier?
10. Is it possible for a dc power supply to have a voltage regulation in excess of 100% using passive loads only? Explain.
11. What are the advantages of a full-wave rectifier over a half-wave rectifier?
12. Show that the ripple factor can be written as:

$$r = \sqrt{\left(\frac{I_{rms}}{I_{dc}}\right)^2 - 1}$$

13. Show that if $R_s = R_f = 0$, one can write for the output voltage of full-wave rectifier as: $v(t) = 2V_m/\pi - (4V_m/3\pi) \cos 2\omega t - (4V_m/5\pi) \cos 4\omega t$; and if R_s and R_f are not negligible, then $v(t) = I(t) R_L$.
14. What is the lowest ripple frequency in a half rectifier and in a full-wave rectifier?
15. Determine the rating of a transformer to deliver 100 Watts of do power to a load under following conditions:
   (i) Half-wave rectifier
   (ii) Full-wave rectifier using two diodes
   (iii) Bridge rectifier.
16. A half-wave rectifier consists of a diode having dynamic resistance of 1 ohm at its operating point and a transformer whose open circuit secondary voltage is 12.6V, 50Hz. It has secondary winding resistance of 3 ohms.
   (a) What is the no load dc voltage of the rectifier?
   (b) What is the output voltage when full load draws a dc current of 100mA?
   (c) What is the percentage voltage regulation of this power supply?
   (d) What is the internal resistance of this power supply?
17. (a) A dc power supply is known to have a ripple factor of 10%. If the dc output voltage is 10V, what is the rms value of output voltage in the output?
   (b) Assuming ripple is approximately sinusoidal in nature, what is the peak-to-peak voltage?
   (c) Assuming that this ripple is approximated as a triangular wave; what is its peak-to-peak voltage?
18. (a) What is the necessary ac input power from the transformer secondary used in a half-wave rectifier to deliver 500W of dc power to the load?
   (b) What is ac input power for the same load in a full-wave rectifier?
19. A 120V, 50Hz voltage is applied to the primary of a 5:1 step-down transformer whose secondary is center-tapped, allowing a load of 1K to be connected to a full-wave rectifier utilizing two diodes. Neglecting the voltage drop across the diodes, determine:
   a. The dc voltage across the load.
   b. The dc current through the load.
   c. The dc power delivered to the load.
   d. The VA rating of the transformer secondary.
   e. The ac input power to the transformer assuming an 80% efficient transformer and ratio of rectification of this circuit of 0.812.
   f. The ripple voltage across the load.
   g. The reading of an ac voltmeter (that responds to peak-to-peak value) connected across the load.

h. The PIV across each diode.

20. Prove that the regulation of both the half-wave and the full-wave rectifier is given by:
% Regulation = R_f / R_L x 100

21. What is a filter? Why is it needed at the output of a rectifier? Describe the CLC or π-filter.

22. A 12.6V center-tapped transformer is used in full-wave rectifier. 100 μF capacitor is used to provide a filtering for a 1K-ohm resistive load. Determine:
(a) The percent ripple in the output
(b) The dc output voltage.

23. An LC filter is to be used to provide a dc output with 1% ripple when operating from a full-wave rectifier at 50Hz. To conserve the size of choke, L/C = 0.01 is recommended (L in henrys, C in microfarads). Determine the required values of L and C.

24. Design a full-wave rectifier with an CLC filter to provide 12V dc at 250mA with a maximum ripple of 50% specify:
(a) Your suggested practical values of L and C.
(b) A bleeder resistor to maintain good voltage regulation.
(c) The transformer secondary voltage assuming the choke has a dc resistance of 10 ohms and bridge rectifier is used.
(d) The PIV capability of the diodes. (e) The peak current capability of the diodes.

25. (a) A π-type CLC filter is to be used at 50Hz to provide 6V dc output with 0.1% ripple for a load of 10K. If the two capacitors are both 50 μF, what must be the minimum value of inductance to use?
(b) Repeat part (a) for a 1K load.

26. A full wave rectifier employs a CLC filter consisting of two 40µF capacitances and a 20H choke. The load current is 50 µA. Calculate the DC output voltage and ripple voltage. The resistance of the choke is 200Ω.

27. The output of a FWR is fed from a 40-0-40 volt transformer. The load current is 0.1 A. Two 40µF capacitors are available. The load resistance is 50 Ω. Calculate the value of inductance for the CLC filter if the ripple factor is 0.0001.

28. Determine the output waveform for the given circuit (fig.2) if
a. input is a sinusoidal wave with a peak voltage of 20V.
b. input is a square wave with a positive peak of 20V and a negative peak of 10V.

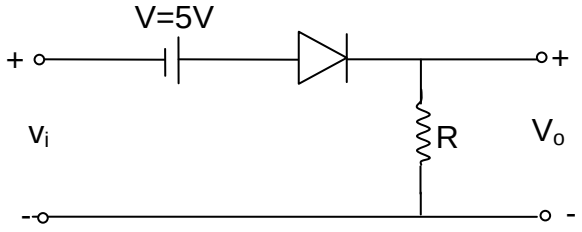


Fig 2

29. Determine Vo for the network shown (fig.3)
a. if the input is a triangular wave of peak voltage 16V.
b. if it is a silicon diode with V_T=0.7V.

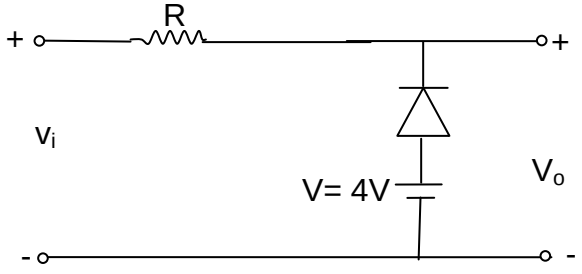


Fig 3

30. What is a clamper? Determine Vo for the network shown in the figure (fig.4) for a square wave input with positive peak of 10V and negative peak of 20V.

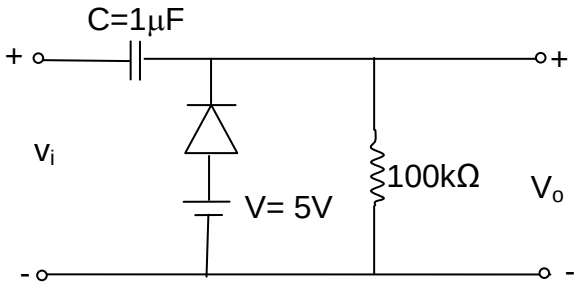


Fig 4

1. What do you mean by a transistor? Explain the working of an npn transistor.
2. What are the basic types of transistor amplifier configuration? What do you understand by active region of operation of a transistor?
3. Define current gain alpha in words and as an equation.
4. Sketch a family of CB output characteristics for a transistor. Indicate the active, cut-off, and saturation regions.
5. Explain Early effect and base width modulation in transistors.
6. (a) Find an expression for I_c for a CB transistor configuration.
   (b) Find an expression for I_c for a CE transistor configuration. Define I_{CBO}.
7. Define β, $h_{FE,}$ I_{CEO}.
8. (a) For a transistor in CE configuration, given that V_{BB} = 5V; R_b = 200K; R_c = 3K; V_{cc} = 10V; β = 100; the transistor is silicon, n-p-n with I_{cc} = 20 nA. Find the transistor currents.
   (a) Repeat part (a) if R_e = 2K emitter resistor is added to the circuit. Also determine if the transistor is in active region.
9. (a) The transistor in CE configuration as in above problem is modified by changing R_b = 50K. Determine whether or not the silicon transistor is in saturation and find I_B and I_C.
   (b) Repeat part (a) above with the 2K-emitter resistance added.
10. Refer to Fig.5. If $\propto$ = 0.98 and V_{BE} = 0.7 V find R_1 in the circuit shown for an emitter current I_E = -2 mA. Neglect the reverse saturation current.

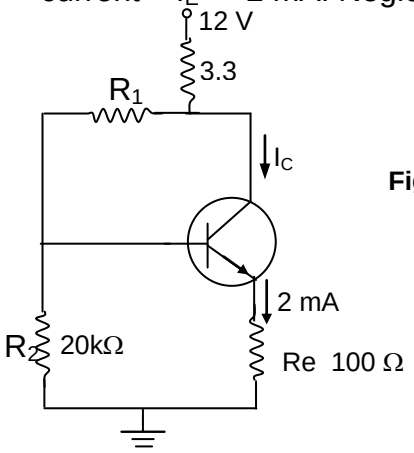


Fig 5

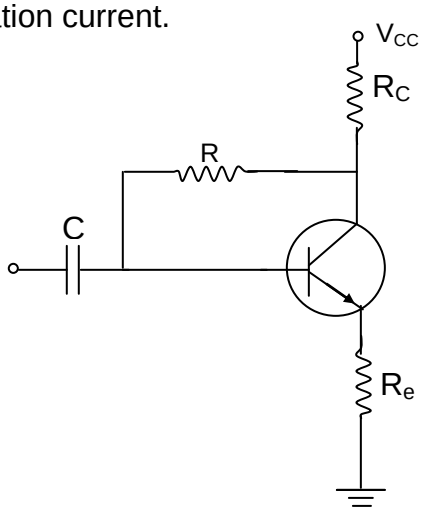


Fig 6

11. Refer to circuit in Fig.6, given that V_{CC} = 24V, R_C = 10K and R_e = 270Ω. If a silicon transistor is used with β = 45 and if V_{CE} = 5V; find R. Neglect reverse saturation current.
12. Derive the relationship between α and β for a transistor.
13. Let I_B = 50μA, I_C = 15 mA, V_{BE} = 0.65V, and V_{CE} = 5V for an npn transistor operating in the active region. Calculate (i) I_E, (ii) V_{CB}, and (iii) the total power dissipated by the transistor.

14. (a) Prove the relation $I_{CEO} = (\beta+1)\, I_{CBO}$
(b) Refer to Fig. (P70). Given that $\beta_{dc} = 75$, $V_{BE} = 0.6V$ $I_{CEO} = 2$ A, $V_{CC} = 4.5V$. Find I_C and V_{CE}.

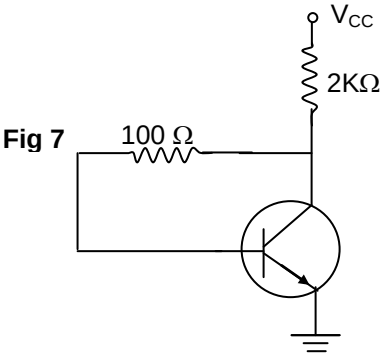


Fig 7

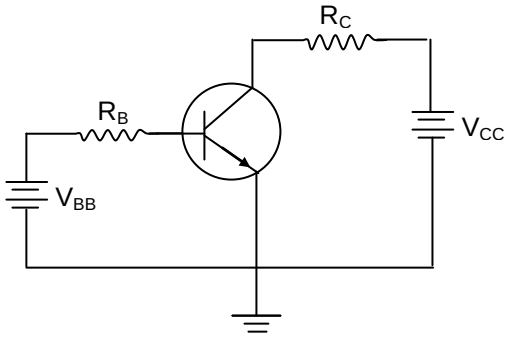


Fig 8

15. Refer to Fig. 8. Given that $\beta_{dc} = 75$, $V_{BE} = 0.6V$, $I_{CEO} = 1.3\mu A$, and $R_{sat} = 40\Omega$ (a) Find α_{dc} and I_{CBO}. Let $V_{BB} = 6V$, $R_B = 27K$, and $V_{CC} = 9V$. (b) Calculate I_C if $R_C = 400$ ohm (c) Find I_C if $R_C = 800$ ohm.
16. (a) What does a dc load line represent?
(b) Can this be used when an ac signal is present?
(c) When is it necessary to draw an ac load line? And, how is it drawn?
17. (a) What is the main advantage of a CE over a CB as far as biasing is concerned?
(b) Why is loading of input signal by the bias resistor not generally a problem in a CE amplifier compared with a CB?
18. (a) What three factors contribute to thermal instability in a CE amplifier? Which one has the least effect in silicon transistors? Why?
(b) What do you understand by the term thermal runaway? Explain in your own words.
19. (a) Define the stability factor S. Find S for a fixed bias CE amplifier and a CB amplifier.
(b) Derive the stability factor S for collector to base bias circuit in a CE amplifier. Discuss the disadvantages of collector to base bias.
(c) Determine the base resistor R_B for collector to base bias and calculate the stability factor S. Given: $V_{CC} = 12V$, $R_L = 330$ ohms; $I_B = 0.3$ mA; $\beta = 100$, $V_{CEQ} = 6V$.
20. (a) Explain how self-bias or emitter bias circuit provides thermal stability.
(b) Derive the expression for the thermal stability factor S for emitter bias.
(c) Determine the bias resistor R_B to provide a bias current of 0.3 mA, for a self-bias circuit. Also calculate the stability factor S, and compare it with the fixed bias circuit. Given: $V_{CC} = 12V$, $R_L = 330$ ohms, $R_e = 100$ ohms, $V_{BE} = 0.2V$; $I_{CQ} = 18$ mA; $\beta = 100$.
21. (a) Draw the circuit for voltage divider bias with emitter bias. This is also known as voltage divider with self-bias. Derive the expression for the stability factor S for this type of bias. Mention its advantages over self-bias.
(b) Explain the function of emitter bypass capacitor. Why is capacitive coupling is used to connect a signal source to an amplifier?
22. In a voltage divider with self-bias circuit R_1 is connected to $+V_{CC}$ and base of the transistor Q. R_2 is connected from base to ground. Determine the values of R_1 and R_2 to provide a bias current $I_B = 0.3$ mA, so as to locate the operating point at $I_{CQ} = 18$ mA and $V_{CEQ} = 4.25V$. $V_{CC} = 12V$. $R_L = 330$ ohms, Re = 100 ohms, $V_{BE} = 0.2V$; $\beta = 100$, Make the stability factor S = 10.
23. The transistor type 2N333 is used in potential divider with emitter bias circuit. The transistor may have any value between 36 and 90 at a temperature of 25^oC. The leakage current I_{CO} has negligible effect on I_C at room temperature. Find R_e, R_1 and R_2 subject to the following specifications:

R_C = 4K, V_{CC} = 20V, nominal bias point is to be at V_{CE} = 10V, I_C = 2mA, and I_C should be in the range 1.75 to 2.25 mA as β varies from 36 to 90. Assume V_{BE} = 0.65V. Note that R_2 is from base to ground.

24. (a) What are the two main types of field-effect transistors? What are the advantages of the FET over a conventional transistor? What do the terms unipolar & bipolar refer to?
    (b) Give basic construction and symbol for the N-channel FET. With help of diagrams explain the principles of operation of the N-channel JEET. Explain self-pinch off.
25. Draw the characteristic curves for the N-channel JEET. Explain channel ohmic region and channel pinch-off region.
26. Define (a) Drain resistance (b) Transconductance (c) I_{DSS}, (d) I_{GSS}, (e) Amplification factor for the FET.
27. (a) Draw the circuit for common source AC amplifier and explain its operation.
    (b)Find the expressions for Av, Ro', Ri', Ci for the circuit in part (a) above.
    (c)For the source follower, give the circuit using p-channel FET and expressions for Av, Ro' and R'i.
28. (a) Give basic construction, symbol, characteristic curves for the N-Channel depletion type MOSFET and explain its operation.
    (b) Repeat part (a) above for the enhancement MOSFET.
    (c) Explain the use of FET as a VVR. Explain voltage-controlled attenuator.
29. If I_{DSS}=4mA, V_P=4V, calculate the quiescent value of I_D, V_{GS} and V_{DS}.
30. An n-channel FET has I_{DSS}=1mA and V_P=-5 V, find the maximum Tran conductance.

1. Draw the hybrid h-parameter equivalent circuit for a linear four terminal network. Write the equations relating input and output variables.
2. Define all the four hybrid h-parameters for a CE-connection. How these parameters can be determined from CE input and output characteristics?
3. Are the h-parameters for transistor constant? What do they vary with? Which ones show greatest variation? What other factors determine the values of a transistor's h-parameters?
4. (a) What are approx conversion formulas for h-parameters from CE values to CC values.
   (b) What are the approx conversion formulas for h-parameters from CE to CB values?
5. Derive the general expressions; valid for CE, CB and CC amplifiers; for the current gain, input resistance; voltage gain, and output resistance.
6. Derive the general expressions for voltage and current gains taking into account the Rg of the source.
7. Consider a CB amplifier with R_L = 1.5 K, Rg = 600 ohms, Vg= 0.15V. The CB, h-parameters are h_{ib} = 20 ohms, $h_{rb} = 3 \times 10^{-4}$, h_{fb} = -0.98, $h_{ob} = 0.5 \times 10^{-6}$ mho. Calculate Ai, Ri, Av, Ro, Ap, Avg and Aig.
8. (a) Show that Ri < h_{ie} in a CE amplifier.
   (b) Show that Ri > h_{ib} in a CE amplifier.
9. The CE h-parameters are h_{ie} = 4K, $h_{re} = 7 \times 10^{-4}$, h_{fe} = 135, hoe = 50μ Siemens. Obtain the CB h-parameters.
10. Draw the approximate hybrid h-parameter equivalent circuit for a CE at low frequencies. Under what conditions this equivalent circuit is valid?
11. Draw the circuit of an emitter follower. List its three most important characteristics.
12. Using approximate h-parameter model for the emitter follower circuit, obtain the expressions for A_I, R_i, A_v and R_o.
13. (a) State Miller's theorem with the aid of a circuit diagram.
    (b) Repeat part (a) above for the dual of Miller's theorem.
13. For the network shown in the figure (fig. 9) determine r_e, Z_i, Z_o, A_v and A_i.

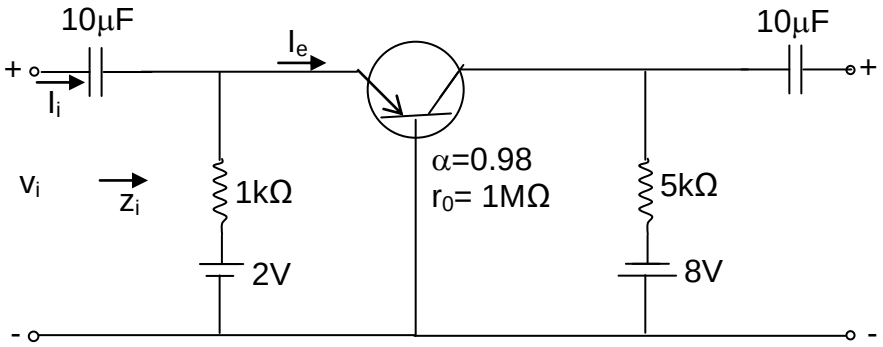
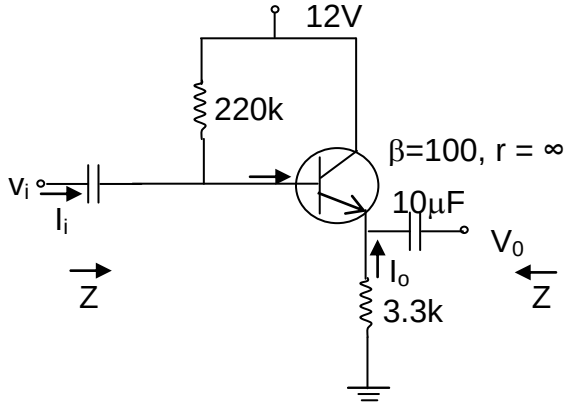


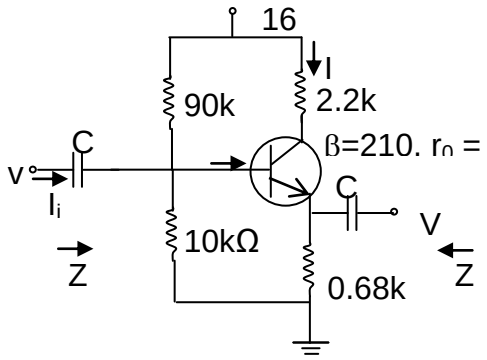
Fig 9

14. For the emitter follower network (fig.10) determine r_e, Z_i, Z_o, A_v and A_i.



Fig

15. For the network shown in the figure (fig.11) determine r_e, Z_i, Z_o, A_v and A_i.



Fig

16. For the network shown in the figure (fig.12) determine Z_i, Z_o, A_v and A_i.

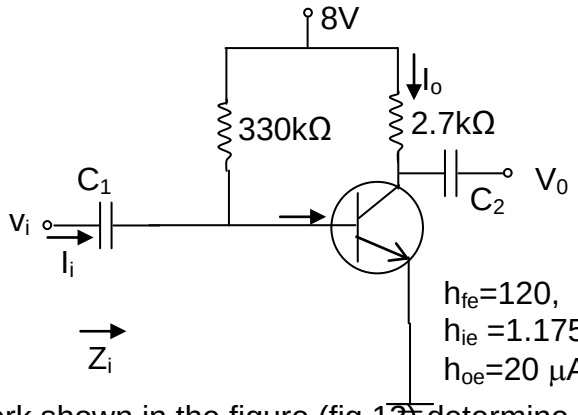


Fig 12

17. For the network shown in the figure (fig.13) determine Z_i, Z_o, A_v and A_i.

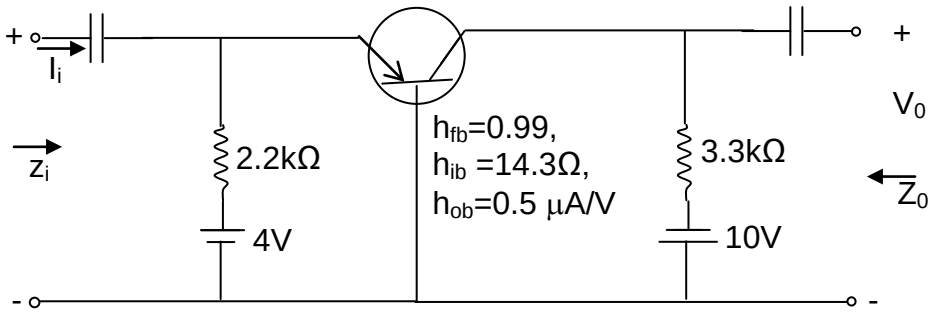


Fig 13

1. What is a power amplifier? What are different types of power amplifier?
2. Draw circuit of a class A power amplifier. Describe its operation with the help of waveforms.
3. (a) Draw circuit of a class A, transformer coupled push-pull amplifier. Describe its operation with the help of waveforms.
   (b) Show that the dc components and all even harmonics are cancelled in this amplifier.
   (c) What other advantages does the push pull configuration provide?
4. Derive the maximum efficiency for a class A power amplifier.
5. Draw the circuit of a class B, transformer coupled, push-pull amplifier. Explain its operation with the help of waveforms.
6. Explain cross-over distortion in class B push-pull amplifiers.
7. Derive an expression for maximum conversion efficiency in class B, push-pull amplifier.
8. Derive an expression for maximum conversion efficiency in class B, push-pull amplifier.
9. Calculate the efficiency of a transformer coupled class A amplifier for a supply of 12V and output of
   a. V_p=12V b. V_p=6V c. V_p=2V.
10. For a class B amplifier using a supply of Vcc=30V and driving a load of 16 Ω, determine the maximum input power, output power and transistor dissipation.
11. Calculate the efficiency of a Class B amplifier for a supply voltage of Vcc=24V with peak output voltage of
    a. $V_{L(p)}$=22V b. $V_{L(p)}$=6V
12. Calculate the harmonic distortion components for an output signal having fundamental amplitude of 2.5 V, second harmonic amplitude of 0.1V and fourth harmonic amplitude of 0.05V.
13. Calculate the total harmonic distortion for the previous problem.
14. For harmonic distortion reading of D_2=0.1, D_3=0.02, D_4=0.01 with I_1=4 A and Rc=8Ω, calculate the total harmonic distortion, fundamental power component and total power.
15. The transistor of a class A power amplifier is supplied from a 6 V battery. If the maximum collector current change is 30μA, find the power transferred to a 8 W loudspeaker when
    (i) it is connected directly to the collector
    (ii) it is coupled through a transformer or maximum power. Also determine the turns ratio for the coupling transformer.
16. For a power transistor working in a class A operation the 0 signal collector current is 100 mA. If dc supply voltage is 12V. Determine
    (i) the maximum ac power output.
    (ii) the power rating of the transistor
    (iii)the maximum collector efficiency.
17. Explain the need for push pull arrangement for power amplifier operation.
18. What is the advantage of Class B complimentary push pull arrangement over simple push pull amplifier?
19. What is crossover distortion? How can it be removed?

20. Prove that a Class B push-pull amplifier produces only odd harmonics.

1. When is Boolean algebra called switching algebra?
2. Obtain the truth table of the function F = xy + xz + yz
3. State and prove the two forms of DeMorgan's Law.
4. Why NAND and NOR gates are called universal?
5. Verify
   (a) AB + ABC + BC = B(C+A)
   (b) AB = ABC + ABC' + ABC
   (c) (A+B)(A+C) = AC + AB
   (d) BC + AC + AB + BCD = BC + AC
6. Simplify the following Boolean functions to minimum number of literals.
   (a) Y(WZ + WZ) + XY
   (b) BC + AC + AB + BCD
   (c) [CD + A] + A + CD + AB
   1. Show that the Boolean expression for the following logic circuit (Fig. 1) is F=(A+B) (C+D) E

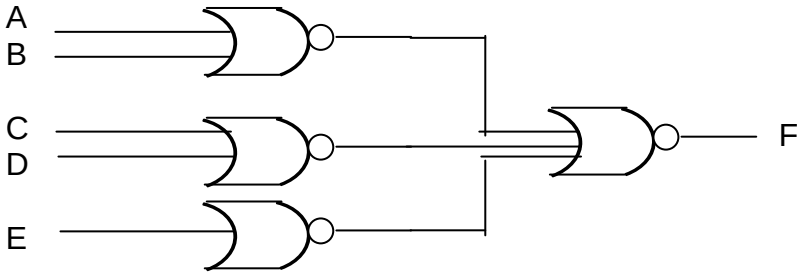


Fig. 1

8. What is the difference between canonical form and standard form? Which form is obtained from a truth table?
9. Define minterms and maxterms for (i) three variables and (ii) four variables.
10. Express F = AB + CD as a canonical
    (i) Sum of Product form (SOP)
    (ii) Product of Sum form (POS)

11. Repeat Q. 10 for the followings.
    (i) X = AB + BC
    (ii) F = r + S(t + r) + St
    (iii) R = (W + X) (Y + Z)
    (iv) T = L + M (NM + ML)
12. Show how NAND gates can be used to build the logic circuit for
    (i) Y = A + BC
    (ii) Y = AB + CD
13. Repeat Q. 12. for NOR gates.
14. Convert the following to other canonical form
    (i) F = $\sum$ (1, 5, 6)
    (ii) F = π (1, 5, 7, 8, 14, 15)
15. Prove that the sum of all minterms of a Boolean function of 3 variables is 1.
16. Prove that the product of all minterms of a Boolean function of 3 variables is 0.
17. Minimize the following switching functions using Karnaugh Map. List all prime implicants and essential prime implicants (nonredundant group).
    (i) F = $\sum$ (1, 3, 5, 6, 7)
    (ii) F = $\sum$ (0, 1, 3, 6, 14, 15) iii) F = π (0, 1, 2, 5, 7, 10, 12)
    (iii) F = π (2, 7, 8, 10, 15) vi) F = $\sum$ (2, 7, 9, 14, 15) + $\sum_d$ (0, 3, (10)
(iv) F = π (5, 7, 9, 10, 15) + π_d (1, 3, 11, 14)

18. Simplify the following non canonical expressions using K– map.
    (i) F = VW + VWY + VWZ
    (ii) F = YZ + WXY + WXY + XYZ
19. Simplify the following Boolean functions by Quine McCluskey Method.
    (i) F = $\sum$ (1, 3, 5, 8, 10, 14)
    (ii) F = $\sum$ (1, 9, 10, 16, 20) + $\sum_d$ (14, 29, 30)
    (iii) F = π (2, 8, 9, 19, 25, 27) + π_d (28, 30).
    (iv) F = $\sum$(0, 8, 14, 19, 31, 52, 58)
20. Give logical design of 2x4 decoders. Realize half adder using above.
21. Show how a full adder can be converted to a full subtractor with the addition of one inverter circuit.
22. One full adder can be realized from two half adder and OR gate. Verify from 1st principle.
23. Repeat Q. 22 for one full subtractor.
24. What are the drawbacks of conventional full adder? How these are minimized in carry look ahead adder?
25. What are the differences between combinational and sequential logic circuits?
26 Explain following with diagram:
    (i) Clocked SR F/F (ii) Clocked J.K. F/F
    (iii) Clocked D F/f (iv) Clocked T F/F
27. Repeat Q.52 to positive and negative edge triggering.
27. Explain the role of present and clear in FLIP-FLOPS.
28. Construct the excitation table and write the characteristic equations for the following FLIP-FLOPS:
    (i) S-R F/F (ii) J-K F/F (iii) T F/F
29. What is race ground condition in J-K F/F? Show how it can be overcome in Master-Slave J-K F/F.
30. Convert an S-R F/F to a J-K F/F waning excitation table.

1. What is an OPAMP? What are the ideal characteristics of an OPAMP?
2. Mention some linear and non-linear applications of OPAMP.
3. Why a feedback is needed in an OPAMP? What type of feedback is used?
4. Derive the expression for output voltage (a) inverting amplifier, (b) Non-inverting amplifier, (c) Differential amplifier, (d) Integrator, (e) Differentiator & (f) Logarithmic amplifier.
5. Derive the expression for exact and ideal input and output impedances of (a) Inverting and (b) Non-inverting amplifier.
6. What do you mean by CMRR? What is its importance? What is its ideal value?
7. Why the two input terminals of an OPAMP with closed loop configuration are thought to be virtually short-circuited?
8. What are the disadvantages of a differential amplifier using single OPAMP? How it can be overcome by using three OPAMPS? Find the expression of voltage gain of such a configuration.
9. For the amplifier shown in Fig. 1, (a) Prove that it acts as DIFF-AMP. (b) Repeat above for double ended CIRCUIT (Fig. 1b).

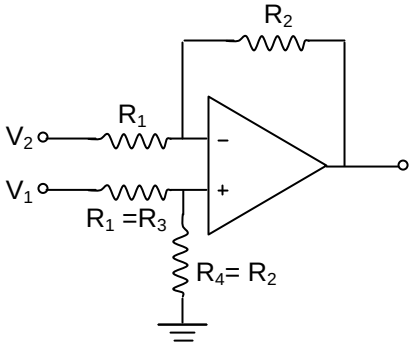


Fig 1 (a)

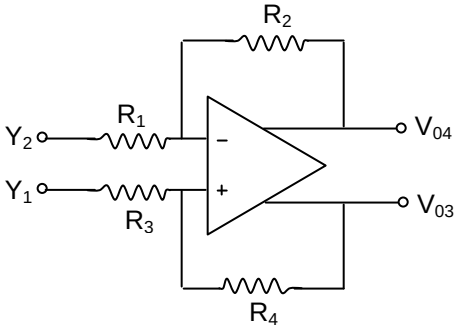


Fig 1 (b)

10. For an OPAMP define the following terms:
    (i) Bandwidth, (ii) CMRR, (iii) Unity gain bandwidth, (iv) Input bias current, (v) Input common mode voltage range, (vi) Input impedance, (vii) Input offset current, (viii) Input offset voltage, (ix) Offset voltage temperature drift, (x) Power supply rejection rate , (xi) Slew rate.
11. Discuss the application of voltage follower.
12. (a) Draw the circuit of an emitter coupled DIFF-AMP.
    (b) Explain why the CMRR $\rightarrow \propto$ for a symmetrical circuit with $R_e \rightarrow \propto$.
13. Derive expression for A_c, A_d and CMRR for symmetrical emitter coupled DIFF-AMP.
14. Explain why the CMRR is infinite if a true constant current source is used in a symmetrical emitter coupled DIFF-AMP.
15. Sketch the transfer characteristics of a DIFF-AMP.
16. Draw an IC OMAMP in block-diagram form and identify each stage by function.
17. Describe the method of measurement of the following quantities of an OPAMP: (i) R_i, (ii) A_v, (iii) R_c, (iv) Slew rate.
18. Show that the exact expression of voltage gain for a non-inverting amplifier is given by $A_{vf} = V_o/ V_{in} = A_v (R_1 + R_f)/ (R_1 + R_f + AR_1)$
19. Show that the exact expression of voltage gain for an inverting amplifier is given by $A_{vf} = V_o/ V_{in} = -A_v R_f)/ (R_1 + R_f + AR_1)$
20. Consider the situation where the inputs to a differential amplifier in the first case is V_x = + 50 μv and V_y = 950 μv. If the CMRR is 100, calculate the outputs in both the cases. Also repeat the problem for CMRR = 10,000