DIGITAL ELECTRONICS LAB
(EC-1412)

LAB MANUAL

IV SEMESTER

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LIST OF EXPERIMENTS:-

1. Study of TTL gates – AND; OR; NOT; NAND; NOR; EX-OR; EX-NOR.

2. Design and realize a given function using K-maps and verify its performance.


4. Implementation of 4x1 multiplexer using Logic Gates.

5. To Design & Verify the Operation of Magnitude Comparator

6. To verify the truth tables of S-R; J-K; T and D type flip flops

7. Design, and Verify the 4- Bit Synchronous Counter

8. Design, and Verify the 4-Bit Asynchronous Counter.

9. To verify the operation of bi-directional shift register.

10. Implementation of 4-Bit Parallel Adder Using 7483 IC
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EXPERIMENT NO: 1

AIM: - Study of TTL gates – AND; OR; NOT; NAND; NOR; EX-OR; EX-NOR

APPARATUS REQUIRED: Power Supply, Digital Trainer Kit., Connecting Leads, IC’s (7400, 7402, 7404, 7408, 7432, and 7486)

BRIEF THEORY:

AND Gate: The AND operation is defined as the output as (1) one if and only if all the inputs are (1) one. 7408 is the two Inputs AND gate IC. A&B are the Input terminals & Y is the Output terminal.

\[ Y = A \cdot B \]

OR Gate: The OR operation is defined as the output as (1) one if one or more than 0 inputs are (1) one. 7432 is the two Input OR gate IC. A&B are the input terminals & Y is the Output terminal.

\[ Y = A + B \]

NOT GATE: The NOT gate is also known as Inverter. It has one input (A) & one output (Y). IC No. is 7404. Its logical equation is,

\[ Y = A \quad \text{NOT} \quad B, \quad Y = A' \]

NAND GATE: The IC no. for NAND gate is 7400. The NOT-AND operation is known as NAND operation. If all inputs are 1 then output produced is 0. NAND gate is inverted AND gate.

\[ Y = (A \cdot B)' \]

NOR Gate: The NOR gate has two or more input signals but only one output signal. IC 7402 is two I/P IC. The NOT- OR operation is known as NOR operation. If all the inputs are 0 then the O/P is 1. NOR gate is inverted OR gate.

\[ Y = (A+B)' \]

EX-OR GATE: The EX-OR gate can have two or more inputs but produce one output. 7486 is two inputs IC. EX-OR gate is not a basic operation & can be performed using basic gates.

\[ Y = A \quad \oplus \quad B \]

LOGIC SYMBOL:

.Logic Symbol of Gates
PROCEDURE:

(a) Fix the IC’s on breadboard & give the supply.
(b) Connect the +ve terminal of supply to pin 14 & -ve to pin 7.
(c) Give input at pin 1, 2 & take output from pin 3. It is same for all except NOT & NOR IC.
(d) For NOR, pin 1 is output & pin 2&3 are inputs.
(e) For NOT, pin 1 is input & p in 2 is output.
(f) Note the values of output for different combination of inputs & draw the TRUTH TABLE.

OBSERVATION TABLE:

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<tr>
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</thead>
<tbody>
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</tr>
</tbody>
</table>

RESULT: We have learnt all the gates ICs according to the IC p in diagram.

PRECAUTIONS:

1. Make the connections according to the IC pin diagram.
2. The connections should be tight.
3. The Vcc and ground should be applied carefully at the specified pin only.

Quiz Questions with answer.

Q.1 Define gates?
Ans. Gates are the digital circuits, which perform a specific type of logical operation.

Q.2 Define IC?
Ans. IC means integrated circuit. It is the integration of no. of components on a common substrate.

Q.3 Give example of Demorgan’s theorem.
Ans. (AB)’ = A’ + B’
(A+B)’ = A’.B’

Q.4 (A+A) A =?
Ans. A.

Q.5. Define Universal gates.
Ans. Universal gates are those gates by using which we can design any type of logical expression.

Q.6 Write the logical equation for AND gate.
Ans. Y = A.B

Q.7 How many no. of input variables can a NOT Gate have?
Ans. One
Q8. Under what conditions the output of a two input AND gate is one?
   Ans. Both the inputs are one.
Q9. 1+0 =?
    Ans. 1
Q10. When will the output of a NAND Gate be 0?
     Ans. When all the inputs are 1.
EXPERIMENT NO: 2

Aim: Design and realize a given function using K-maps and verify its performance.

APPARATUS REQUIRED: Power Supply, Digital Trainer, IC’s (7404, 7408, 7432) Connecting leads.

BRIEF THEORY: Karnaugh maps are the most extensively used tool for simplification of Boolean functions. It is mostly used for functions having up to six variables beyond which it becomes very cumbersome. In an n-variable K-map there are 2^n cells. Each cell corresponds to one of the combination of n variable, since there are 2^n combinations of n-variables. Gray code has been used for the identification of cells.

Example- \( f(A, B, C, D) = A'BC + AB'C + ABC + ABC \) (SOP)

Reduced form is \( BC + AC + AB \) and POS form is \( f(X, Y, Z) = Y' (X' + Y + Z') (X + Z) \)

LOGIC DIAGRAM

PROCEDURE:

(a) With given equation in SOP/POS forms first of all draw a K-map.
(b) Enter the values of the O/P variable in each cell corresponding to its Min/Max term.
(c) Make group of adjacent ones.
(d) From group write the minimized equation.
(e) Design the ckt. of minimized equation & verify the truth table.

RESULT/CONCLUSION: Implementation of SOP and POS form is obtained with AND and OR gates.

PRECAUTIONS:
1) Make the connections according to the IC pin diagram.
2) The connections should be tight.
3) The \( V_{cc} \) and ground should be applied carefully at the specified pin only.
**Quiz Questions with answer.**

Q.1 Define K-map?
Ans. It is a method of simplifying Boolean Functions in a systematic mathematical way.

Q.2 Define SOP?
Ans. Sum of Product.

Q.3 Define POS?
Ans. Product of Sum.

Q.4 What are combinational circuits?
Ans. These are those circuits whose output depends upon the inputs present at that instant of time.

Q.5 What are sequential circuits?
Ans. These are those circuits whose output depends upon the input present at that time as well as the previous output.

Q.6 If there are four variables how many cells the K-map will have?
Ans. 16.

Q.7 When two min-terms can be adjacent?
Ans. $2^n$.

Q.8 Which code is used for the identification of cells?

Q.9 Define Byte?
Ans. Byte is a combination of 8 bits.

Q.10 When simplified with Boolean Algebra $(x + y)(x + z)$ simplifies to
Ans. $x + yz$
EXPERIMENT NO: 3

Aim:- Implementation and Verification of Decoder/De-Multiplexer and Encoder using Logic Gates.

APPARATUS REQUIRED: IC 7447, 7-segment display, IC 74139 and connecting leads.

BRIEF THEORY:

ENCODER: An encoder is a device, circuit, transducer, software program, algorithm or person that converts information from one format or code to another, for the purposes of standardization, speed, secrecy, security, or saving space by shrinking size. An encoder has M input and N output lines. Out of M input lines only one is activated at a time and produces equivalent code on output N lines. If a device output code has fewer bits than the input code has, the device is usually called an encoder. For example Octal-to-Binary Encoder take 8 inputs and provides 3 outputs, thus doing the opposite of what the 3-to-8 decoder does. At any one time, only one input line has a value of 1. The figure below shows the truth table of an Octal-to-binary encoder.

For an 8-to-3 binary encoder with inputs I0-I7 the logic expressions of the outputs Y0-Y2 are:

\[ Y0 = I1 + I3 + I5 + I7 \]
\[ Y1 = I2 + I3 + I6 + I7 \]
\[ Y2 = I4 + I5 + I6 + I7 \]

DECODER: A decoder is a device which does the reverse operation of an encoder, undoing the encoding so that the original information can be retrieved. The same method used to encode is usually just reversed in order to decode. It is a combinational circuit that converts binary information from n input lines to a maximum of \(2^n\) unique output lines. In digital electronics, a decoder can take the form of a multiple- input, multiple-output logic circuit that converts coded inputs into coded outputs, where the input and output codes are different. e.g. n-to-\(2^n\), binary-coded decimal decoders. Enable inputs must be on for the decoder to function, otherwise its outputs assume a single "disabled" output code word. In case of decoding all combinations of three bits eight (\(2^3=8\)) decoding gates are required. This type of decoder is called 3-8 decoder because 3 inputs and 8 outputs. For any input combination decoder outputs are 1.

DEMULTIPLEXER: Demultiplexer means generally one into many. A demultiplexer is a logic circuit with one input and many outputs. By applying control signals, we can steer the input signal to one of the output lines. The circuit has one input signal, m control signal and n output signals. Where \(2^n = m\). It functions as an electronic switch to route an incoming data signal to one of several outputs.
LOGIC DIAGRAM:

3:8 Decoder  Octal to Binary Encoder

PROCEDURE:
1) Connect the circuit as shown in figure.
2) Apply Vcc & ground signal to every IC.
3) Observe the input & output according to the truth table.
OBSERVATION TABLE:

Truth table for Decoder

<table>
<thead>
<tr>
<th>Inputs</th>
<th>Outputs</th>
</tr>
</thead>
<tbody>
<tr>
<td>a</td>
<td>b</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
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<td>1</td>
<td>1</td>
</tr>
</tbody>
</table>

Output function: \( \overline{a} \overline{b} c \quad \overline{a} b \overline{c} \quad \overline{a} b c \quad a \overline{b} c \quad \overline{a} b \overline{c} \quad a b \overline{c} \quad a b c \quad \overline{a} b c \quad a b c \)

Truth table for Encoder

Truth table for Demux

RESULT: Encoder/ decoder and demultiplexer have been studied and verified.

PRECAUTIONS:

1) Make the connections according to the IC pin diagram.
2) The connections should be tight.
3) The Vcc and ground should be applied carefully at the specified pin only.
Quiz Questions with answer.

Q. 1 What do you understand by decoder?
Ans. A decoder is a combinational circuit that converts binary information from n input lines to a maximum of 2n unique output lines. Most IC decoders include one or more enable inputs to control the circuit operation.

Q. 2 What is demultiplexer?
Ans. The demultiplexer is the inverse of the multiplexer, in that it takes a single data input and n address inputs. It has $2^n$ outputs. The address input determine which data output is going to have the same value as the data input. The other data outputs will have the value 0.

Q. 3 What do you understand by encoder?
Ans. An encoder or multiplexer is therefore a digital IC that outputs a digital code based on which of its several digital inputs is enabled.

Q. 4 What is the main difference between decoder and demultiplexer?
Ans. In decoder we have n input lines as in demultiplexer we have n select lines.

Q. 5 Why Binary is different from Gray code?
Ans. Gray code has a unique property that any two adjacent gray codes differ by only a single bit.

Q. 6 Write down the method of Binary to Gray conversion.
Ans. Using the Ex-Or gates.

Q. 7 Convert 0101 to Decimal.
Ans. 5

Q. 8 Write the full form of ASCII Codes?

Q. 9 If a register containing 0.110011 is logically added to register containing 0.101010 what would be the result?
Ans. 111011

Q. 10 Binary code is a weighted code or not?
Ans. Yes
EXPERIMENT NO : 4

Aim: Implementation of 4x1 Multiplexer using Logic Gates.

APPARATUS REQUIRED: Power Supply, Digital Trainer, Connecting Leads, IC’s 74153(4x1 multiplexer).

BRIEF THEORY:

MULTIPLEXER: Multiplexer generally means many into one. A multiplexer is a circuit with many inputs but only one output. By applying control signals we can steer any input to the output. The fig. (1) shows the general idea. The ckt. has n-input signal, control signal & one output signal. Where $2^n = m$. One of the popular multiplexer is the 16 to 1 multiplexer, which has 16 input bits, 4 control bits & 1 output bit.

PIN CONFIGURATION:

IC 74153 (4x1 multiplexer)

LOGIC DIAGRAM:

Multiplexer (4x1) IC 74153
PROCEDURE:
1. Fix the IC's on the bread board & give the input supply.
2. Make connection according to the circuit.
3. Give select signal and strobe signal at respective pins.
4. Connect +5 v Vcc supply at pin no 24 & GND at pin no 12.
5. Verify the truth table for various inputs.

OBSERVATION TABLE:

Truth Table of multiplexer (4x1) IC 74153

<table>
<thead>
<tr>
<th>A</th>
<th>B</th>
<th>C0</th>
<th>C1</th>
<th>C2</th>
<th>C3</th>
<th>G</th>
<th>Y</th>
</tr>
</thead>
<tbody>
<tr>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>1</td>
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<td>X</td>
<td>1</td>
<td>0</td>
<td>1</td>
</tr>
</tbody>
</table>

RESULT: Verify the truth table of multiplexer for various inputs.

PRECAUTIONS:

1) Make the connections according to the IC pin diagram.
2) The connections should be tight.
3) The Vcc and ground should be applied carefully at the specified pin only.

Quiz Questions with answer.

Q.1 Why is MUX called as “Data Selector”?
Ans. This selects one out of many inputs.

Q.2 What do you mean by Multiplexing?
Ans. Multiplexing means selecting only a single input out of many inputs.

Q.3 What is Digital Multiplexer?
Ans. The multiplexer which acts on digital data.

Q.4 What is the function of Enable input to any IC?
Ans. When this enable signal is activated.

Q.5 What is demultiplexer?
Ans. A demultiplexer transmits the data from a single source to various sources.

Q.6 Can a decoder function as a D’MUX?
Ans. Yes

Q.7 What is the role of select lines in a Demultiplexer?
Ans. Select line selects the output line.
Q.8 Differentiate between functions of MUX & D’MUX?
Ans. Multiplexer has only single output but demultiplexer has many outputs.
Q.9 The number of control lines required for a 1:8 demultiplexer will be
Ans. 3
Q.10 How many 4:1 multiplexers will be required to design 8:1 multiplexer?
Ans. 2
EXPERIMENT NO: 5

Aim: - To Design & Verify the Operation of Magnitude Comparator

APPARATUS REQUIRED: Power Supply, Digital Trainer Kit., Connecting Leads, and IC’s (7404, 7408, 7485 and 7486).

BRIEF THEORY: Comparator compares the value of signal at the input. It can be designed to compare many bits. The adjoining figure shows the block diagram of comparator. Here it receives to two 2-bit numbers at the input & the comparison is at the output.

CIRCUIT DIAGRAM:

![Comparator Circuit Diagram]

PROCEDURE:
   a. Make the connections according to the circuit diagram.
   b. The output is high if both the inputs are equal.
   c. Verify the truth table for different values.

OBSERVATION TABLE:

<table>
<thead>
<tr>
<th>P0</th>
<th>Q0</th>
<th>P1</th>
<th>Q1</th>
<th>LOW IF P IS NOT EQUAL TO Q</th>
<th>HIGH IF Q IS EQUAL TO Q</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>HIGH</td>
<td>HIGH</td>
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<tr>
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<tr>
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<td>1</td>
<td>0</td>
<td>1</td>
<td>LOW</td>
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<tr>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>LOW</td>
<td></td>
</tr>
</tbody>
</table>
4-bit Comparator

<table>
<thead>
<tr>
<th>A_3 B_3</th>
<th>A_2 B_2</th>
<th>A_1 B_1</th>
<th>A_0 B_0</th>
<th>A&gt;B</th>
<th>A=B</th>
<th>A&gt;B</th>
<th>A=B</th>
<th>A&gt;B</th>
<th>A=B</th>
<th>A&lt;B</th>
</tr>
</thead>
<tbody>
<tr>
<td>A_3&gt;B_3</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
</tr>
<tr>
<td>A_3&lt;B_3</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
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</tr>
<tr>
<td>A_3=B_3</td>
<td>A_2&gt;B_2</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
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<td>X</td>
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</tr>
<tr>
<td>A_3=B_3</td>
<td>A_2&lt;B_2</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
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<td>X</td>
</tr>
<tr>
<td>A_3=B_3</td>
<td>A_2=B_2</td>
<td>A_1&gt;B_1</td>
<td>X</td>
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<td>A_2=B_2</td>
<td>A_1=B_1</td>
<td>A_0&gt;B_0</td>
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</table>

RESULT: The comparator is designed & verified.
**PRECAUTIONS:**
1) Make the connections according to the IC pin diagram.
2) The connections should be tight.
3) The Vcc and ground should be applied carefully at the specified pin only.

**Quiz Questions with answer.**

Q1. What is comparator?
Ans. Comparator compares the inputs (bits).

Q2. What are universal gates?
Ans. NAND, NOR.

Q3. What is the full form of BCD?
Ans. Binary Coded decimal.

Q4. What is the base of binary number system?
Ans. 2

Q5. How many bits are there in one byte?
Ans. 8

Q6. How many digits are there in octal number system?
Ans. 8

Q7. What is the binary no. equivalent to decimal no. 20?
Ans. 10100

Q8. How decimal no. minus 7 can be represented by 4 bit signed binary no’s?
Ans. 1111

Q9. Convert the octal no 67 into binary no.?
Ans. 110111

Q10. A binary digit is called?
Ans. Bit.
EXPERIMENT NO: 6

Aim: To verify the truth tables of S-R; J-K; T and D type flip flops

APPARATUS REQUIRED: IC’S 7400, 7402 & 7476 Digital Trainer & Connecting leads.

BRIEF THEORY:

• **RS FLIP-FLOP:** There are two inputs to the flip-flop defined as R and S. When I/Ps R = 0 and S = 0 then O/P remains unchanged. When I/Ps R = 0 and S = 1 the flip-flop is switches to the stable state where O/P is 1 i.e. SET. The I/P condition is R = 1 and S = 0 the flip-flop is switched to the stable state where O/P is 0 i.e. RESET. The I/P condition is R = 1 and S = 1 the flip-flop is switched to the stable state where O/P is forbidden.

• **JK FLIP-FLOP:** For purpose of counting, the JK flip-flop is the ideal element to use. The variable J and K are called control I/Ps because they determine what the flip-flop does when a positive edge arrives. When J and K are both 0s, both AND gates are disabled and Q retains its last value.

• **D FLIP-FLOP:** This kind of flip flop prevents the value of D from reaching the Q output until clock pulses occur. When the clock is low, both AND gates are disabled D can change value without affecting the value of Q. On the other hand, when the clock is high, both AND gates are enabled. In this case, Q is forced to equal the value of D. When the clock again goes low, Q retains or stores the last value of D. a D flip flop is a bistable circuit whose D input is transferred to the output after a clock pulse is received.

• **T FLIP-FLOP:** The T or "toggle" flip-flop changes its output on each clock edge, giving an output which is half the frequency of the signal to the T input. It is useful for constructing binary counters, frequency dividers, and general binary addition devices. It can be made from a J-K flip-flop by tying both of its inputs high.

CIRCUIT DIAGRAM:

SR Flip Flop

![SR Flip Flop Diagram]

D Flip Flop
PROCEDURE:
1. Connect the circuit as shown in figure.
2. Apply Vcc & ground signal to every IC.
3. Observe the input & output according to the truth table.

TRUTH TABLE:
SR FLIP FLOP:

<table>
<thead>
<tr>
<th>CLOCK</th>
<th>S</th>
<th>R</th>
<th>( Q_{n+1} )</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
<td>NO CHANGE</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>?</td>
</tr>
</tbody>
</table>

D FLIPFLOP:

<table>
<thead>
<tr>
<th>INPUT</th>
<th>OUTPUT</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
</tr>
</tbody>
</table>

JK FLIPFLOP

<table>
<thead>
<tr>
<th>CLOCK</th>
<th>S</th>
<th>R</th>
<th>( Q_{n+1} )</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
<td>NO CHANGE</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>( Q_n' )</td>
</tr>
</tbody>
</table>
T FLIP FLOP

<table>
<thead>
<tr>
<th>CLOCK</th>
<th>S</th>
<th>R</th>
<th>( Q_{n+1} )</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
<td>NO CHANGE</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
<td>( Q_n' )</td>
</tr>
</tbody>
</table>

RESULT: Truth table is verified on digital trainer.

PRECAUTIONS:

1) Make the connections according to the IC pin diagram.
2) The connections should be tight.
3) The \( V_{cc} \) and ground should be applied carefully at the specified pin only.

Quiz Questions with answer.

Q 1. Flip flop is Astable or Bistable?
Ans. Bistable.

Q2. What are the I/Ps of JK flip–flop where this race round condition occurs?
Ans. Both the inputs are 1.

Q3. When RS flip-flop is said to be in a SET state?
Ans. When the output is 1.

Q4. When RS flip-flop is said to be in a RESET state?
Ans. When the output is 0.

Q5. What is the truth table of JK flip-flop?

<table>
<thead>
<tr>
<th>J</th>
<th>K</th>
<th>( Q_{n+1} )</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>( Q_n )</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>( Q_n )</td>
</tr>
</tbody>
</table>

Q6. What is the function of clock signal in flip-flop?
Ans. To get the output at known time.

Q7. What is the advantage of JK flip-flop over RS flip-flop?
Ans. In RS flip-flop when both the inputs are 1 output is undetermined.

Q8. In D flip-flop I/P = 0 what is O/P?
Ans. 0

Q9. In D flip-flop I/P = 1 what is O/P?
Ans. 1

Q10. In T flip-flop I/P = 1 what is O/P?
Ans. \( Q_n \)
EXPERIMENT NO: 7

Aim: – Design, and Verify the 4-Bit Synchronous Counter

APPARATUS REQUIRED: Digital trainer kit and 4 JK flip flop each IC 7476 (i.e. dual JK flip flop) and two AND gates IC 7408.

BRIEF THEORY: Counter is a circuit which cycle through state sequence. Two types of counter, Synchronous counter (e.g. parallel) and Asynchronous counter (e.g. ripple). In Ripple counters same flip-flop output to be used as clock signal source for other flip-flop. Synchronous counter use the same clock signal for all flip-flop.

PIN CONFIGURATION:
Dual JK Master Slave Flip Flop with clear & preset

LOGIC DIAGRAM:
4-Bit Synchronous counter

Clock
<table>
<thead>
<tr>
<th>Pin Number</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Clock 1 Input</td>
</tr>
<tr>
<td>2</td>
<td>Preset 1 Input</td>
</tr>
<tr>
<td>3</td>
<td>Clear 1 Input</td>
</tr>
<tr>
<td>4</td>
<td>J1 Input</td>
</tr>
<tr>
<td>5</td>
<td>Vcc</td>
</tr>
<tr>
<td>6</td>
<td>Clock 2 Input</td>
</tr>
<tr>
<td>7</td>
<td>Preset 2 Input</td>
</tr>
<tr>
<td>8</td>
<td>Clear 2 Input</td>
</tr>
<tr>
<td>9</td>
<td>J2 Input</td>
</tr>
<tr>
<td>10</td>
<td>Complement Q2 Output</td>
</tr>
<tr>
<td>11</td>
<td>Q2 Output</td>
</tr>
<tr>
<td>12</td>
<td>K2 Input</td>
</tr>
<tr>
<td>13</td>
<td>Ground</td>
</tr>
<tr>
<td>14</td>
<td>Complement Q1 Output</td>
</tr>
<tr>
<td>15</td>
<td>Q1 Output</td>
</tr>
<tr>
<td>16</td>
<td>K1 Input</td>
</tr>
</tbody>
</table>

**OBSERVATION TABLE:**

<table>
<thead>
<tr>
<th>States</th>
<th>Count</th>
</tr>
</thead>
<tbody>
<tr>
<td>(0_4)</td>
<td>(0_3)</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
</tr>
</tbody>
</table>
PROCEDURE:
   a) Make the connections as per the logic diagram.
   b) Connect +5v and ground according to pin configuration.
   c) Apply diff combinations of inputs to the i/p terminals.
   d) Note o/p for summation.
   e) Verify the truth table.

RESULT:  4-bit synchronous counter studied and verified.

PRECAUTIONS:
   1. Make the connections according to the IC pin diagram.
   2. The connections should be tight.
   3. The Vcc and ground should be applied carefully at the specified pin only.

Quiz Questions with answer.

Q.1 What do you understand by counter?
Ans. Counter is a register which counts the sequence in binary form.

Q.2 What is asynchronous counter?
Ans. Clock input is applied to LSB FF. The output of first FF is connected as clock to next FF.

Q.3 What is synchronous counter?
Ans. Where Clock input is common to all FF.

Q.4 Which flip flop is used in asynchronous counter?
Ans. All Flip-Flops are toggling FF.

Q.5 Which flip flop is used in synchronous counter?
Ans. Any FF can be used.

Q.6 What do you understand by modulus?
Ans. The total no. of states in counter is called as modulus. If counter is modulus-n, then it has n different states.

Q.7 What do you understand by state diagram?
Ans. State diagram of counter is a pictorial representation of counter states directed by arrows in graph.

Q.8 What do you understand by up/down counter?
Ans. Up/Down Synchronous Counter: two way counter which able to count up or down.
Q.9 Why Asynchronous counter is known as ripple counter?
Ans. Asynchronous Counter: flip-flop doesn’t change condition simultaneously because it doesn’t use single clock signal Also known as ripple counter because clock signal input as ripple through counter.
Q.10 which type of counter is used in traffic signal?
Ans. Down counters.

EXPERIMENT NO: 8
Aim: – Design, and Verify the 4-Bit Asynchronous Counter.

APPARATUS REQUIRED: Digital trainer kit and 4 JK flip flop each IC 7476 (i.e dual JK flip flop) and two AND gates IC 7408.

BRIEF THEORY: Counter is a circuit which cycle through state sequence. Two types of counter, Synchronous counter (e.g. parallel) and Asynchronous counter (e.g. ripple). In Ripple counter same flip-flop output to be used as clock signal source for other flip-flop. Synchronous counter use the same clock signal for all flip-flop.

PIN CONFIGURATION:

![Pin diagram of JK M/S Flip Flop](image)

LOGIC DIAGRAM: 4-Bit Asynchronous counter

<table>
<thead>
<tr>
<th>Pin Number</th>
<th>Description</th>
</tr>
</thead>
</table>

![Logic Diagram](image)
<table>
<thead>
<tr>
<th></th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Clock 1 Input</td>
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<td>11</td>
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<tr>
<td>12</td>
<td>K2 Input</td>
</tr>
<tr>
<td>13</td>
<td>Ground</td>
</tr>
<tr>
<td>14</td>
<td>Complement Q1 Output</td>
</tr>
<tr>
<td>15</td>
<td>Q1 Output</td>
</tr>
<tr>
<td>16</td>
<td>K1 Input</td>
</tr>
</tbody>
</table>

**PROCEDURE:**

a) Make the connections as per the logic diagram.
b) Connect +5v and ground according to pin configuration.
c) Apply diff combinations of inputs to the i/p terminals.
d) Note o/p for summation.
e) Verify the truth table.

**RESULT:** 4-bit asynchronous counter studied and verified.

**PRECAUTIONS:**

1. Make the connections according to the IC pin diagram.
2. The connections should be tight.
3. The Vcc and ground should be applied carefully at the specified pin only.

**Quiz Questions with answer.**

Q.1 How many flip-flops are required to make a MOD-32 binary counter?
   Ans. 5.
Q.2 The terminal count of a modulus-11 binary counter is _______.
   Ans. 1010.
Q.3 Synchronous counters eliminate the delay problems encountered with asynchronous counters because the:
   Ans. Input clock pulses are applied simultaneously to each stage.
Q.4. Synchronous construction reduces the delay time of a counter to the delay of:
   Ans. a single flip-flop and a gate.
Q5. What is the difference between a 7490 and a 7492?

Ans. 7490 is a MOD-10, 7492 is a MOD-12.

Q6. When two counters are cascaded, the overall MOD number is equal to the _______ of their individual MOD numbers.

Ans. Product.

Q7. A BCD counter is a _______.

Ans. decade counter.

Q8. What decimal value is required to produce an output at "X"?

Ans. 5.

Q9. How many AND gates would be required to completely decode ALL the states of a MOD-64 counter, and how many inputs must each AND gate have?

Ans. 64 gates, 6 inputs to each gate.

Q10. A ring counter consisting of five Flip-Flops will have ______ states.

Ans. 5 states.
EXPERIMENT NO - 9

Aim – To verify the operation of bi-directional shift register.

Apparatus Required: -- Digital trainer kit, IC 7495, Connecting wires etc.

Brief Theory:
A bidirectional shift register is one in which the data can be shifted either left or right. It can be implemented by using gate logic that enables the transfer of a data bit from one stage to the next stage to the right or to the left, depending on the level of a control line. A 4-bit bidirectional shift register is shown in Figure below. A HIGH on the RIGHT / LEFT control input allows data bits inside the register to be shifted to the right, and a LOW enables data bits inside the register to be shifted to the left.

Procedure:-

Serial In Parallel Out (SIPO):

1. Connections are made as per circuit diagram.
2. Apply the data at serial i/p
3. Apply one clock pulse at clock 1 (Right Shift) observe this data at QA.
4. Apply the next data at serial i/p.
5. Apply one clock pulse at clock 2, observe that the data on QA will shift to QB and the new data applied will appear at QA.
6. Repeat steps 2 and 3 till all the 4 bits data are entered one by one into the shift register.

Serial In Serial Out (SISO):

1. Connections are made as per circuit diagram.
2. Load the shift register with 4 bits of data one by one serially.
3. At the end of 4th clock pulse the first data ‘d0’ appears at QD.
4. Apply another clock pulse; the second data ‘d1’ appears at QD.
5. Apply another clock pulse; the third data appears at QD.
6. Application of next clock pulse will enable the 4th data ‘d3’ to appear at QD. Thus the data applied serially at the input comes out serially at QD.

Parallel In Serial Out (PISO):

1. Connections are made as per circuit diagram.
2. Apply the desired 4 bit data at A, B, C and D.
3. Keeping the mode control M=1 apply one clock pulse. The data applied at A, B, C and D will appear at QA, QB, QC and QD respectively.
4. Now mode control M=0. Apply clock pulses one by one and observe the Data coming out serially at QD

**Parallel In Parallel Out (PIPO):**

1. Connections are made as per circuit diagram.
2. Apply the 4 bit data at A, B, C and D.
3. Apply one clock pulse at Clock 2 (Note: Mode control M=1).
4. The 4 bit data at A, B, C and D appears at QA, QB, QC and QD respectively.

**PIN CONFIGURATION**

![SIPO (Right Shift)](image)
RESULT: 4-bit bidirectional shift register is studied and verified.
EXPERIMENT NO - 10

Aim – Implementation of 4-Bit Parallel Adder Using 7483 Ic.

APPARATUS REQUIRED – Digital trainer kit, IC 7483 (4-bit parallel adder).

BRIEF THEORY - A 4-bit adder is a circuit which adds two 4-bits numbers, say, A and B. In addition, a 4-bit adder will have another single-bit input which is added to the two numbers called the carry-in (C_in). The output of the 4-bit adder is a 4-bit sum (S) and a carry-out (C_out) bit.

PIN CONFIGURATION–
Pin Diagram of IC 7483

LOGIC DIAGRAM:-

7483 4-bit Parallel Adder
OBSERVATION TABLE –

Truth table of 4-bit parallel adder

<table>
<thead>
<tr>
<th>A3</th>
<th>A2</th>
<th>A1</th>
<th>A0</th>
<th>B3</th>
<th>B2</th>
<th>B1</th>
<th>B0</th>
<th>C4 (V)</th>
<th>S3(V)</th>
<th>S2(V)</th>
<th>S1(V)</th>
<th>S0(V)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0 0</td>
<td>0 1</td>
<td>0 0</td>
<td>1 0</td>
<td>0 0</td>
<td>1 0</td>
<td>0 0</td>
<td>0 0</td>
<td>1 1</td>
<td>0 0</td>
<td>0 0</td>
<td>0 0</td>
<td></td>
</tr>
<tr>
<td>0 1</td>
<td>0 1</td>
<td>1 1</td>
<td>0 0</td>
<td>1 1</td>
<td>1 1</td>
<td>1 0</td>
<td>0 0</td>
<td>0 0</td>
<td>0 0</td>
<td>0 0</td>
<td></td>
<td></td>
</tr>
<tr>
<td>1 0</td>
<td>1 0</td>
<td>0 1</td>
<td>0 1</td>
<td>0 1</td>
<td>0 1</td>
<td>0 1</td>
<td>0 0</td>
<td>1 0</td>
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<td></td>
<td></td>
</tr>
<tr>
<td>1 1</td>
<td>1 1</td>
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<td>1 1</td>
<td>1 1</td>
<td>1 1</td>
<td>1 1</td>
<td>1 0</td>
<td>1 1</td>
<td>1 0</td>
<td>0 0</td>
<td>0 0</td>
<td></td>
</tr>
</tbody>
</table>

PROCEDURE –
- a) Make the connections as per the logic diagram.
- b) Connect +5v and ground according to pin configuration.
- c) Apply diff combinations of inputs to the i/p terminals.
- d) Note o/p for summation.
- e) Verify the truth table.

RESULT- Binary 4-bit full adder is studied and verified.

PRECAUTIONS:
1. Make the connections according to the IC pin diagram.
2. The connections should be tight.
3. The Vcc and ground should be applied carefully at the specified pin only.

Quiz Questions with answer.

Q1 What do you understand by parallel adder?
Ans. If we place full adders in parallel, we can add two- or four-digit numbers or any other size desired i.e. known as parallel adder.

Q2 What happens when an N-bit adder adds two numbers whose sum is greater than or equal to $2^N$?
Ans. Overflow.

Q3 Is Excess-3 code is weighted code or not?
Ans. Excess-3 is not a weighted code.

Q4 What is IC no. of parallel adder?
Ans. IC 7483.

Q5 What is the difference between Excess-3 & Natural BCD code?
Ans. Natural BCD code is weighted code but Excess-3 code is not weighted code.

Q6 What is the Excess-3 code for $(396)_{10}$?
Ans. $(396)_{10} = (011011001001)_{EX-3}$

Q7 Can we obtain 1’s complement using parallel adder?
Ans. Yes

Q8 Can we obtain 2’s complement using parallel adder?
Ans. yes

Q9 How many bits can be added using IC7483 parallel adder?
Ans. 4 bits.

Q10 Can you obtain subtractor using parallel adder?
Ans. Yes