Parallel Adder Continues:

Advantages of a parallel adder

- Since the operation is parallel and simultaneous, the time required to complete the operation is independent of the number of bits.
- Hence they are also faster than their serial counterparts.
- It is cheaper.

Disadvantages of a parallel adder

Each adder receives inputs to their A and B ports instantaneously. However, the carry ports don't get their inputs till the earlier adder are done finishing their operation. This introduces a delay.

This delay adds up as the number of full adders increases.

Serial Adder

The **serial binary adder** or **bit-serial adder** is a digital circuit that performs binary addition bit by bit. The serial full adder has three single-bit inputs for the numbers to be added and the carry in. There are two single-bit outputs for the sum and carry out. The carry-in signal is the previously calculated carry-out signal. The addition is performed by adding each bit, lowest to highest, one per clock cycle.

A serial adder consists of a 1-bit full-adder and several shift registers. In serial adders, pairs of bits are added simultaneously during each clock cycle. Two right-shift registers are used to hold the numbers (*A* and *B*) to be added, while one left-shift register is used to hold the sum (*S*).

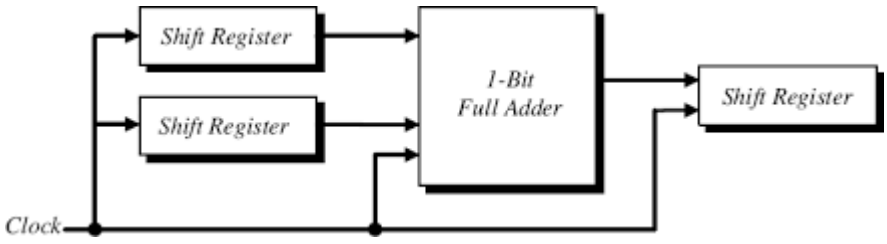


Fig:1 Block Diagram of serial Adder

A finite-state machine adder performs the addition operation on the values stored in the input shift registers and stores the sum in a separate shift register during several clock cycles. During each clock cycle, two input bits a_i and b_i are shifted from the two input right-shift registers into the 1-bit full-adder, which adds the two bits and evaluates the sum bit s_i and the carryout bit ci_{+1}. The sum bit s_i, is shifted out to the left-shift register and the carryout bit ci_{+1} is stored in the state

memory of the serial adder for the next two bits. The time sequence of the operation of a 4-bit serial adder is illustrated in Figure 2.

A	B	S	s_i	c_{i+1}
1011	0011	0000	0	1
0101	0001	1000	1	1
0010	0000	1100	1	0
0001	0000	1110	1	0

Fig:2 Time Sequence of the Operation of a 4-bit Serial Adder

Difference between Serial Adder and Parallel Adder

Serial Adder	Parallel Adder
1. Serial Adder is less fast	1. Parallel Adder is generally faster
2. It requires fewer components	2. It requires more components compared to serial adder
3. Addition is performed bit by bit starting from the LSB	3. All the bits are added simultaneously

Ripple Carry Adder:

In digital electronics adding of two-bit binary numbers can be possible by using half adder. And if the input sequence has a three-bit sequence, then the addition process can be completed by using a full adder. But if the numbers of bits are more in the input sequence then the process can be completed by using half adder. Because full adder cannot be able to complete the addition operation. So these drawbacks can be overcome by using "Ripple Carry Adder". It's a unique type of logic circuit used for adding the N-bit numbers in digital operations. This article describes an overview of what is ripple-carry-adder and its operation.

A structure of multiple full adders is cascaded in a manner to gives the results of the addition of an n bit binary sequence. This adder includes cascaded full adders in its structure so, the carry will be generated at every full adder stage in a ripple-carry adder circuit. These carry output at each full adder stage is forwarded to its next full adder and there applied as a carry input to it. This process continues up to its last full adder stage. So, each carry output bit is rippled to the next stage of a full adder. By this reason, it is named as "RIPPLE CARRY ADDER". The most important feature of it is to add the input bit sequences whether the sequence is 4 bit or 5 bit or any.

“One of the most important point to be considered in this carry adder is the final output is known only after the carry outputs are generated by each full adder stage and forwarded to its next stage. So there will be a delay to get the result with using of this carry adder”.

4-bit Ripple Carry Adder

The below diagram represents the 4-bit ripple-carry adder. In this adder, four full adders are connected in cascade. Co is the carry input bit and it is zero always. When this input carry ‘Co’ is applied to the two input sequences A1 A2 A3 A4 and B1 B2 B3 B4 then output represented with S1 S2 S3 S4 and output carry C4.

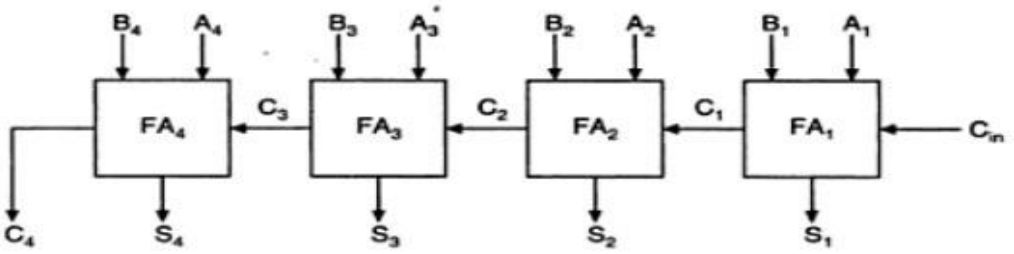


Fig: 4-bit ripple carry adder diagram

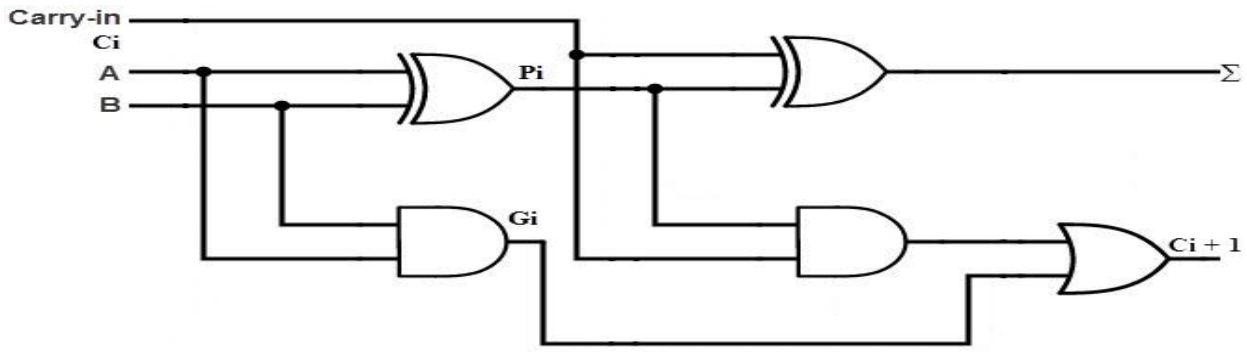
Working of 4-bit Ripple Carry Adder

- Let’s take an example of two input sequences 0101 and 1010. These are representing the A4 A3 A2 A1 and B4 B3 B2 B1.
- As per this adder concept, input carry is 0.
- When Ao & Bo are applied at 1st full adder along with input carry 0.
- Here A1 =1 ; B1=0 ; Cin=0
- Sum (S1) and carry (C1) will be generated as per the Sum and Carry equations of this adder. As per its theory, the output equation for the Sum = A1⊕B1⊕Cin and Carry = A1B1⊕B1Cin⊕CinA1
- As per this equation, for 1st full adder S1 =1 and Carry output i.e., C1=0.
- Same like for next input bits A2 and B2, output S2 = 1 and C2 = 0. Here the important point is the second stage full adder gets input carry i.e., C1 which is the output carry of initial stage full adder.
- Like this will get the final output sequence (S4 S3 S2 S1) = (1 1 1 1) and Output carry C4 = 0
- This is the addition process for 4-bit input sequences when it’s applied to this carry adder.

Carry Look-Ahead Adder:

A carry-Lookahead adder is a fast parallel adder as it reduces the propagation delay by more complex hardware, hence it is costlier. In this design, the carry logic over fixed groups of bits of

the adder is reduced to two-level logic, which is nothing but a transformation of the ripple carry design. This method makes use of logic gates so as to look at the lower order bits of the augend and addend to see whether a higher order carry is to be generated or not. Let us discuss in detail.



A	B	Ci	C i +1	Condition
0	0	0	0	No carry generate
0	0	1	0	
0	1	0	0	
0	1	1	1	No carry propagate
1	0	0	0	
1	0	1	1	
1	1	0	1	Carry generate
1	1	1	1	

Consider the full adder circuit shown above with corresponding truth table. If we define two variables as carry generate Gi and carry propagate Pi then,

$$P_i = A_i \oplus B_i$$

$$Gi = Ai\ Bi$$

The sum output and carry output can be expressed as

$$Si = Pi \oplus Ci$$

$$C\ i +1 = Gi + Pi\ Ci$$

Where Gi is a carry generate which produces the carry when both Ai, Bi are one regardless of the input carry. Pi is a carry propagate and it is associate with the propagation of carry from Ci to Ci +1.

The carry output Boolean function of each stage in a 4 stage carry-Lookahead adder can be expressed as

$$C1 = G0 + P0\ Cin$$

$$C2 = G1 + P1\ C1$$

$$= G1 + P1\ G0 + P1\ P0\ Cin$$

$$C3 = G2 + P2\ C2$$

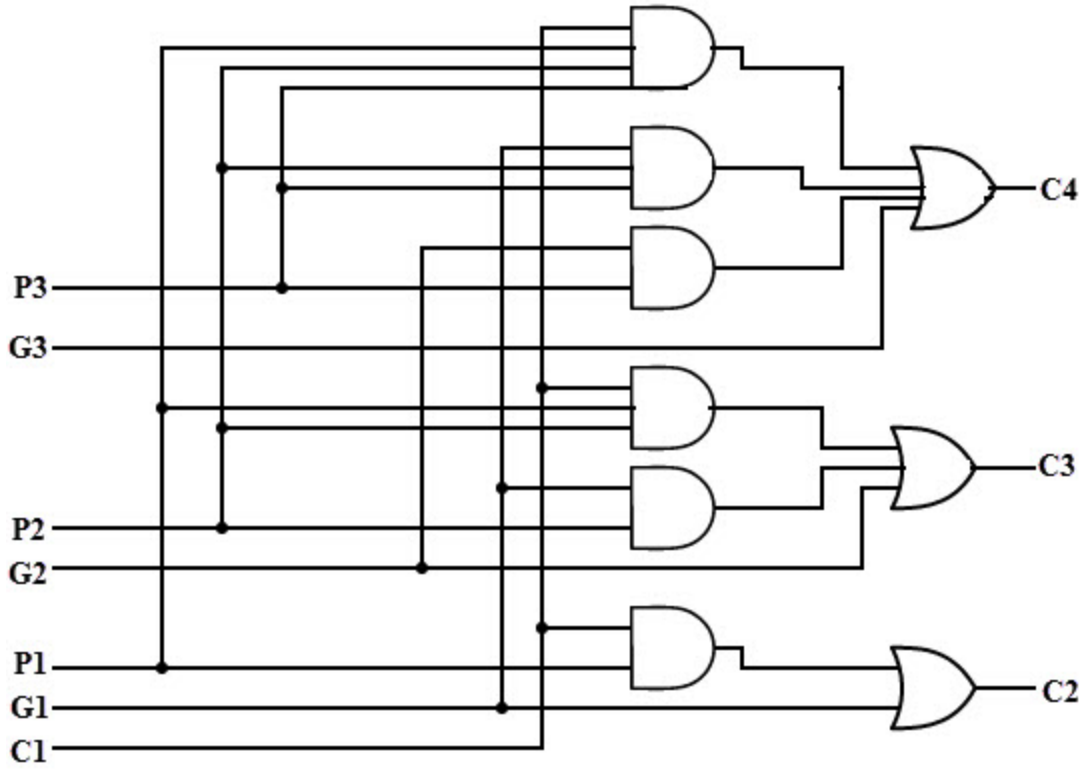
$$= G2 + P2\ G1 + P2\ P1\ G0 + P2\ P1\ P0\ Cin$$

$$C4 = G3 + P3\ C3$$

$$= G3 + P3\ G2 + P3\ P2\ G1 + P3\ P2\ P1\ G0 + P3\ P2\ P1\ P0\ Cin$$

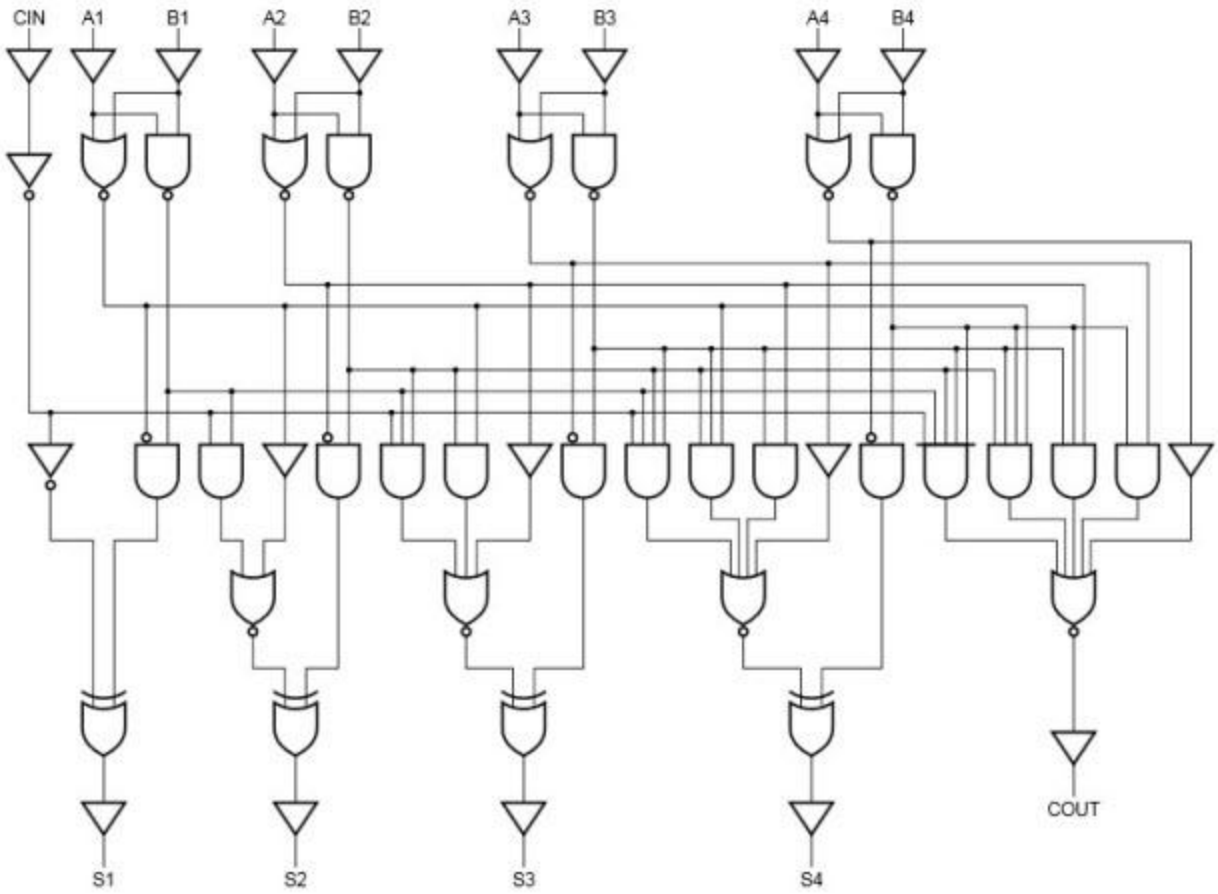
From the above Boolean equations we can observe that C4 does not have to wait for C3 and C2 to propagate but actually C4 is propagated at the same time as C3 and C2. Since the Boolean expression for each carry output is the sum of products so these can be implemented with one level of AND gates followed by an OR gate.

The implementation of three Boolean functions for each carry output (C2, C3 and C4) for a carry-Lookahead carry generator shown in below figure.



Therefore, a 4 bit parallel adder can be implemented with the carry-Lookahead scheme to increase the speed of binary addition as shown in below figure. In this, two Ex-OR gates are required by each sum output. The first Ex-OR gate generates Pi variable output and the AND gate generates Gi variable.

Hence, in two gates levels all these P's and G's are generated. The carry-Lookahead generators allows all these P and G signals to propagate after they settle into their steady state values and produces the output carriers at a delay of two levels of gates. Therefore, the sum outputs S2 to S4 have equal propagation delay times.



It is also possible to construct 16 bit and 32 bit parallel adders by cascading the number of 4 bit adders with carry logic. A 16 bit carry-Lookahead adder is constructed by cascading the four 4 bit adders with two more gate delays, whereas the 32 bit carry-Lookahead adder is formed by cascading of two 16 bit adders.

In a 16 bit carry-Lookahead adder, 5 and 8 gate delays are required to get C16 and S15 respectively, which are less as compared to the 9 and 10 gate delay for C16 and S15 respectively in cascaded four bit carry-Lookahead adder blocks. Similarly, in 32 bit adder, 7 and 10 gate delays are required by C32 and S31 which are less compared to 18 and 17 gate delays for the same outputs if the 32 bit adder is implemented by eight 4 bit adders.

Advantages of Carry Look Ahead Adder-

The advantages of carry look ahead adder are-

- It generates the carry-in for each full adder simultaneously.
- It reduces the propagation delay.

Disadvantages of Carry Look Ahead Adder-

The disadvantages of carry look ahead adder are-

- It involves complex hardware.
- It is costlier since it involves complex hardware.
- It gets more complicated as the number of bits increases.