Answer the following questions:

1. Why is the clock cycle time for pipelined execution is more than the same for unpipelined execution?
2. Explain the three limitations of loop unrolling?
3. Explain the pros and cons of deeper pipelining used in MIPS R4000.
4. What is the purpose of TC stage in 8-stage pipeline of MIPS R4000?
5. What is superpipelining? What are its benefits and limitations?
6. What is superscalar processor? What are its benefits and limitations?
7. Give example of code that would cause WAR and WAW hazards?
8. What is meant by instruction level parallelism (ILP)? How does it differ from thread level parallelism (TLP)?
9. What is static approach of exploiting ILP?
10. What is dynamic approach of exploiting ILP?
11. Explain whether you would prefer static approach or dynamic approach of exploiting ILP?
12. What is ARM processor? Give short history of evolution of ARM processor.
13. List some computer hardware where ARM processors are used?
14. Why is it easier to implement instruction pipeline in RISC machines in comparison with CISC machines?
15. What are delayed branch and its delay slot? How does it reduce the branch hazard?
16. Suppose there is no limitation of main memory size. One does not mind increase in code size due to loop unrolling. Would you prefer fully (or as much as possible) unrolled code in this situation in order to speed up the execution of instruction? Explain.
17. How would you unroll the loop ***m*** times if it iterates ***k*** times where ***k*** is a variable?
18. What is scoreboard used in CDC 6600 computer? How does it handles various data hazards and structural hazard?
19. What is the limitation of scoreboard?
20. Does the scoreboard technique of dynamic exploitation of ILP ensure precise exception?
21. What is an exception in the context of program code execution?
22. What is meant by a precise exception? Why is it required?