NATIONAL INSTITUTE OF TECHNOLOGY JAMSHEDPUR
JHARKHAND – 831014

Department of Computer Applications

AUTUMN SEMESTER 2021-2022

Course Handout

Date: 18/10/2021

Course No. **: CA3102**

Course title **: Computer Organization & Architecture**

Instructor-in-charge **: ASHOK KUMAR MEHTA**

Course description

Number systems, Integer and floating point representation, Character codes (ASCII, EBCDIC), Error detection & correction codes.
Boolean Algebra and logic gates, Combinational circuits.
Flip-Flops, Finite state machines, State table diagrams, state minimization, Decoders, Multiplexers, Registers, Counters**,** PAL, PLA and gate array.
Stack organization, Instruction formats, Addressing modes, Instruction types, Instruction cycle and execution cycle.
Hardwired control, Micro-programmed control, RISC, CISC, Pipelining in CPU design, Superscalar processors.
Storage technologies, Memory array organization, Memory hierarchy, Interleaving, cache and virtual memories.
Input-output processing, bus interface, Data transfer techniques, I/O interrupts, channels.

Scope

- To provide a good fundamental concepts of Computer Organization & Architecture
- To focus on the major components of Computer System
- To make proficient in Computer Organization & Architecture

Objectives

- At the end of this course, the students will be able to understand the structure and behavior of the various functional modules of the Computer and how they interact to provide the processing needs of the user.
- At the end of this course, the students will be able to design and implement Computer Organization & Architecture.

Text books

T1. M. Morris Mano, "Computer System and Architecture", Pearson Education.

Reference books

R1. John P. Hayes, "Computer Architecture and Organization", McGraw-Hill International Edition.

R2. C. Hamacher, Z. Vranesic, S. Zaky"Computer Organization", McGraw-Hill International Edition.

Course plan

Lecture No.	Learning objectives	Topics to be covered	Refer to Chapter, See (Book)
1-3	Number systems, Integer and floating point representation, Character codes (ASCII, EBCDIC)	Number systems	3 (T1)
4	Error detection & correction codes	Error detection & correction codes	3 (T1)
5-7	Boolean Algebra and logic gates, Combinational circuits	Combinational circuits	1 (T1)
8-10	Flip-Flops	Flip-Flops	1 (T1)
11-13	Finite state machines, State table diagrams, state minimization	Finite state machines	1 (T1)
14-15	Decoders, Multiplexers, PAL, PLA and gate array	Digital Components	2 (R1)
16-19	Registers, Counters	Registers	7 (T1)
20-23	Stack organization, Instruction formats, Addressing modes, Instruction types	Instruction	8 (T1)
24-25	Instruction cycle and execution cycle	Instruction cycle	5 (T1)
26-28	Hardwired control, Micro-programmed control	Control unit	5,7 (T1)
29-30	RISC, CISC, Pipelining in CPU design, Superscalar processors	CPU design	5 (R1)
31-34	Storage technologies, Memory array organization, Memory hierarchy	Memory	6 (R1)
35-39	Interleaving, cache and virtual memories	High speed memory	12 (T1)
40-44	Input-output processing, bus interface, Data transfer techniques, I/O interrupts, channels	Input-Output Organization	11(T1)

Evaluation Scheme

EC No.	Evaluation Component	Duration	Weightage	Date & Time	Nature of the component
1	Mid Sem	2 Hrs	30%	To be anounced	Closed Book
2	End Sem Exam.	3 Hrs	50%	To be anounced	Closed Book
3	Assignment & Attendance		20%	Submit by 18.01.2022	Take Home

Chamber consultation hour: Tuesday, 5.00 to 6.00 PM

Notices: All notices regarding the course will be displayed only on the **Department of Computer Applications notice board**.

Instructor In-Charge
CA3102